Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled)
2. (canceled)
3. (canceled)
4. (canceled)
5. (canceled)
6. (canceled)
7. (canceled)
8. (canceled)
9. (canceled)
10. (canceled)
11. (canceled)
12. (canceled)
13. (canceled)
14. (canceled)
15. (canceled)
16. (canceled)
17. (canceled)
18. (canceled)
19. (canceled)

20. (Currently amended) ~~The~~ A fabrication process ~~according to any of claims 9, 14 and 18~~ for making an enhanced avalanche ruggedness Fast Recovery Diode, the process comprising:

selecting a semiconductor material of a first dopant type;

patterning and introducing a first dopant of a second type opposite in polarity to the first dopant type into the top surface of the semiconductor material at a peripheral region of the device;

diffusing said first dopant to create field spreading structures for blocking reverse voltage;

introducing a second dopant of the first type into a central portion of the semiconductor material top surface;

diffusing said second dopant to create a region with enhanced doping concentration of the first type within the semiconductor material in the central portion of the device;

introducing and diffusing a third dopant of the second type to a predetermined depth within said enhanced doping region to form a main PN junction and effect a lower avalanche breakdown in the central portion in relationship to a periphery of the main PN junction; and

forming metal electrodes on the top surface and a backside of the semiconductor material to conduct current through the diode;

further comprising a blanket implant of the first dopant type into the semiconductor surface to counter the effect of counter-doping and compensation by ~~the~~ a life-time control dopant.

21. (canceled)

22. (Currently amended) ~~The~~ A fabrication process ~~according to any of claims 9, 14 and 18~~ for making an enhanced avalanche ruggedness Fast Recovery Diode, the process comprising:

selecting a semiconductor material of a first dopant type;

patterning and introducing a first dopant of a second type opposite in polarity to the first dopant type into the top surface of the semiconductor material at a peripheral region of the device;

diffusing said first dopant to create field spreading structures for blocking reverse voltage;

introducing a second dopant of the first type into a central portion of the semiconductor material top surface;

diffusing said second dopant to create a region with enhanced doping concentration of the first type within the semiconductor material in the central portion of the device;

introducing and diffusing a third dopant of the second type to a predetermined depth within said enhanced doping region to form a main PN junction and effect a lower avalanche breakdown in the central portion in relationship to a periphery of the main PN junction; and

forming metal electrodes on the top surface and a backside of the semiconductor material to conduct current through the diode;

further comprising a first deep life-time control dopant profile having a gradient that is higher in doping concentration toward the backside of the semiconductor; and

a second shallow life-time control profile having a gradient that is heavier toward the top surface forming a shallow gradient band of decreasing concentration near the PN junction.

23. (Currently amended) The fabrication process according to claim ~~17~~ 20 further comprising a first deep life-time control dopant profile having a gradient that is higher in doping concentration toward the backside of the semiconductor; and

a second shallow life-time control profile having a gradient that is heavier toward the top surface forming a shallow gradient band of decreasing concentration near the PN junction.

24. (canceled)

25. (canceled)

26. (canceled)

27. (Currently amended) A fabrication process ~~according to claim 9~~ for making an enhanced avalanche ruggedness Fast Recovery Diode, ~~including~~ comprising:

selecting a semiconductor material of a first dopant type;

introducing a preliminary dopant of ~~the~~ a first type prior to ~~the~~ a step of patterning and introducing ~~the~~ a first dopant of ~~the~~ a second type to prevent current flow along a surface of the semiconductor material between an active area and an edge of the device across the field-spreading structures.;

diffusing said first dopant to create field spreading structures for blocking reverse voltage;

introducing a second dopant of the first type into a central portion of the semiconductor material top surface;

diffusing said second dopant to create a region with enhanced doping concentration of the first type within the semiconductor material in the central portion of the device;

introducing and diffusing a third dopant of the second type to a predetermined depth within said enhanced doping region to form a main PN junction and effect a lower avalanche breakdown in the central portion in relationship to a periphery of the main PN junction; and

completing the device by forming metal electrodes on the top surface and a backside of the semiconductor material to conduct current through the diode.

28. (New) A fabrication process according to any of claims 20, 22, and 27 wherein the concentration of the second dopant of the first type is in the range of 1.0E15 to 5.0E17 /cm3 and a diffusion depth of 3 to10 um.

29. (New) A fabrication process according to any of claims 20, 22, and 27 wherein the concentration of the third dopant of the second type is in the range of 1.0E16 to 5.0E18 /cm3 and a diffusion depth of 2 to 6 um.

30. (New) A fabrication process according to any of claims 20, 22, and 27 wherein an amount of additional charge contained between the second dopant of the first type and a starting epitaxial layer is in the range of 1.0E11 to 1.0E13 /cm2.

31. (New) A fabrication process according to any of claims 20, 22, and 27 including introducing and diffusing life-time control dopant into the semiconductor to control device speed.

32. (New) The fabrication process according to any of claims 20, 22 and 27 in which the semiconductor material comprises a lightly doped epitaxial layer on top of a heavily doped substrate.

33. (New) A fabrication process according to any of claims 20, 22, and 27 wherein the PN junction is formed by a body diffusion of a MOS gate-controlled device.

34. (New) A fabrication process according to any of claims 20, 22, and 27 wherein the PN junction is a deeply placed P+ diffusion underneath a body diffusion in a MOS gate-controlled device.

35. (New) A fabrication process according to any of claims 20, 22, and 27 including irradiating the semiconductor to effect a life-time control to control device speed.

36. (New) A fabrication process for making a Fast Recovery Diode, the process comprising:

selecting a semiconductor material of a first dopant type;

patterning and introducing dopant of a second type opposite in polarity to the first dopant type into the top surface of the semiconductor material;

diffusing said dopant of a second type to create field spreading structures for blocking reverse voltage and to form a main PN junction in the central active portion of the device;

forming metal electrodes on the top surface and a backside of the semiconductor material to conduct current through the diode;

further comprising a blanket implant of a dopant of the first dopant type into the semiconductor surface to counter the effect of counter-doping and compensation by a life-time control dopant.

37. (New) A fabrication process for making a Fast Recovery Diode, comprising:

selecting a semiconductor material of a first dopant type;

introducing a preliminary dopant of the first type prior to a step of patterning and introducing a first dopant of a second type opposite in polarity to the first dopant type to prevent current flow along a surface of the semiconductor material between an active area and an edge of the device across the field-spreading structures;

diffusing said first dopant to create field spreading structures for blocking reverse voltage;

patterning and introducing dopant of a second type opposite in polarity to the first dopant type into the top surface of the semiconductor material;

diffusing said dopant of a second type to create field spreading structures for blocking reverse voltage and to form a main PN junction in the central active portion of the device; and

completing the device by forming metal electrodes on the top surface and a backside of the semiconductor material to conduct current through the diode.

38. (New) The fabrication process according to claim 36 or 37 further comprising a first deep life-time control dopant profile having a gradient that is higher in doping concentration toward the backside of the semiconductor; and

a second shallow life-time control profile having a gradient that is heavier toward the top surface forming a shallow gradient band of decreasing concentration near the PN junction.